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FROM: Peter S. Zawilski

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RE:	**SERIAL NO.**	**09/775,370**
	DOCKET NO.	**PHA 51108A**

39 Pages (including cover sheet)

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Appeal Brief in Triplicate (3 x 12 pgs.)

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/775,370
Filing Date	02/01/2001
First Named Inventor	Tammy Zheng
Group Art Unit	2826
Examiner Name	Leonardo Andujar
Total Number of Pages In This Submission: 38	Attorney Docket Number: PHA 51108A

ENCLOSURES *(check all that apply)*

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- [ ] Response to Missing Parts/ Incomplete Application
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☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 320

Complete if Known	
Application Number	09/775,370
Filing Date	2/1/2001
First Named Inventor	Tammy Zheng
Examiner Name	Leonardo Andujar
Art Unit	2826
Attorney Docket No.	PHA 51108A

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FEE CALCULATION

1. BASIC FILING FEE

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1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

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2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims			Fee from below	Fee Paid
Total Claims		-20** =		X	=
Independent Claims		-3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	320
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

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SUBMITTED BY				(Complete *if applicable*)	
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Signature	Peter Zawilski			*Date*	27-JAN-2003

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13/Appeal Brief P. Walker 1-30-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Tammy Zheng *et al.*
Serial No. 09/775,370
Filed: February 1, 2001
For: Semiconductor Device Comprising Aluminum-Based Plugs Between First and Second Metal Portions

Patent Application
Examiner: Leonardo Andujar
Group: 2826
Docket No.: PHA 51108A

APPEAL BRIEF

Assistant Commissioner for Patents & Trademarks
Washington, DC 20231

Sir:

This is an Appeal Brief submitted pursuant to 37 CFR §1.1.92 for the above-referenced patent application and is being filed in triplicate.

I. REAL PARTY IN INTEREST

The real party in interest is Koninklijke Philips Electronics NV (KPENV); a corporation organized under the laws of The Netherlands. The patent application had been assigned to VLSI Technology, Inc. (VLSI); a corporation organized under the laws of the State of Delaware and having a principal place of business in San Jose, California. VLSI had been acquired by KPENV in June of 1999 through its sister division, Philips Electronics North America Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 27 - 37 are being appealed.

IV. STATUS OF AMENDMENTS

Upon filing of the application on February 1, 2001, Appellant submitted a Preliminary Amendment to replace claims 1 – 26 with new claims 27 – 46. In response to the first Non-Final Office Action Restriction Requirement dated November 20, 2001, Appellant filed a Response and Amendment dated December 20, 2001, canceling claims 38 – 46 without traverse and electing claims 27 – 37. In response to second Non-Final Office Action dated February 27, 2002, Appellant filed a Response and Amendment dated May 28, 2002, making changes to the Specification and Drawings and amending claims. In response to the Final Office Action dated August 27, 2002, Appellant filed a Response and Amendment dated October 28, 2002, making changes to the Title and Drawings.

An Advisory Action dated November 6, 2002 indicated the After Final Response did not place the application in condition for allowance. In response to the Advisory Action, Appellant filed a Notice of Appeal on November 27, 2002 and is now presenting this Appeal Brief.

The claims as finally amended are attached hereto as an Appendix.

V. SUMMARY OF INVENTION

The present invention is generally directed to the manufacture of a semiconductor device. In particular, the invention relates to prevention of the formation of voids in metal plugs that connect metal interconnect lines at different levels. In an example embodiment, a semiconductor device comprises a first metal portion (210) over a substrate, a dielectric layer (230) about the first metal portion and a second metal portion (255) above the dielectric layer (230). (Refer to FIGS. 2A – 2D and the discussion on pages 8 – 14 of the Specification). A single-layer aluminum alloy plug (240) extends from the first metal portion (210) through the dielectric layer (230) to the second metal portion (255). The plug has a first upper surface extending laterally beyond the second metal portion (255) and substantially planar to an upper surface of the dielectric layer (230) and a second upper surface that extends above the first upper surface.

VI. ISSUES FOR REVIEW

Claims 27 – 37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Korman* (US 5,959,357) in view of *Green et al.* (US 4,851,895).

Claims 28 – 32 and 34 stand rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Claims 28 – 30 and 34 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The issues are a follows:

1. **Is the §103(a) rejection of the claims proper when the asserted *Korman*'357 and *Green* '895 references fail to teach or suggest every element of the claimed invention and therefore, the Examiner failed to establish a *prima facie* case of obviousness?**

2. **Is the §103(a) rejection of the claims proper when hindsight is applied in view of the combination of the asserted teachings provided by way of the *Korman*'357 and *Green* '895 references?**

3. **Is the §103(a) rejection of the claims proper when the asserted modification of the primary *Korman*'357 reference would render that reference unsatisfactory for its intended purpose?**

4. **Is the §112(1) rejection proper when the Specification describes the claimed subject matter in such a manner that one skilled in the art would be able to make and use the invention?**

5. **Is the §112(2) rejection proper even though the Specification is concluded with claims particularly pointing out and distinctly claiming the subject matter which the Appellants regard as their invention?**

VII. GROUPING OF CLAIMS

The claims as now presented stand and fall together.

VIII. ARGUMENT

A. Scope and Content of the Prior Art.

Korman (US 5,959,357) titled, "FET Array for Operation at Different Power Levels" relates generally to field effect transistors. The present invention is directed to an arrangement of three or more metallization layers for the source, drain and gate terminals of one or more off-the-shelf field-effect transistors (FETs) to form a package that compensates for the high resistance of its polycrystalline silicon gate electrodes and provides a high-level of circuit performance having an optimum balance between conduction (resistance) and switching (capacitance) losses.

Green et al. (US 4,851,895) titled, "Metallization for Integrated Devices" is concerned with electrical contacts and conductors and their manufacture in integrated device technology. Integrated device metallizations are produced from a ruthenium material. More specifically, an integrated device comprises a conductive region in which conduction is essentially confined, for some distance, to a material which consists of at least 40 atom percent ruthenium. Such material can be used as gate metallization, source metallization, drain metallization, as a diffusion barrier, and as an interconnect metallization. A particular advantage arises from the fact that electrical conductivity of a layer remains high when ruthenium is oxidized to ruthenium dioxide, and such oxidation may indeed be intentional in view of particular suitability of ruthenium dioxide as a diffusion barrier material.

B. Discussion of the Issues.

ISSUE 1: The §103(a) rejection of the claims is improper when the asserted *Korman*'357 and *Green* '895 references fail to teach or suggest every element of the claimed invention and; therefore, the Examiner failed to establish a *prima facie* case of obviousness

The §103(a) rejection must be reversed because the cited references fail to teach or suggest every element of the claimed invention and, therefore, fail to meet all of the criteria for a *prima facie* case of obviousness. As indicated in the M.P.E.P., a §103(a) rejection requires that the cited references teach or suggest all of the limitations of the

rejected claims and that there be motivation for modifying the primary *Korman*'357 reference to arrive at the presently-claimed invention. In the present instance, Appellants submit that the cited portions of the references fail to teach or suggest every element of the claimed invention. For instance, the "single layer plug 42b" asserted by the Examiner (*see* Office Actions of 2/27/2002 and 8/27/2002) appears to be a two-layer plug. Specifically, Applicant submits that a lower portion of the "single layer plug 42b" below surface 42c would apparently have to be formed prior to an upper portion thereof that is above the surface 42c because the upper portion of the plug is tapered at surface 42c. As column 5, lines 36-39 and FIG. 3 of the '357 reference indicate, the portion "single layer plug 42b" is in fact comprised of separate vias 46. Moreover, the Examiner does not assert, nor does it appear, that the first upper surface 42c is substantially planar to an upper surface of the dielectric layer 44. In view of the above, the Examiner has failed to assert a reference or references that teach or suggest all of the limitations of independent claim 27. Furthermore, because the remaining rejected claims depend from claim 27, these dependent claims also include limitations for which the Examiner has failed to provide a reference showing teaching or suggestion thereof. However, Appellants submit that the Examiner's assertion that the "single layer plug 42b" is a single layer is misplaced when in fact, the "single layer plug 42b" includes multiple vias 46, as discussed above and acknowledged by the Examiner in his Office Actions. Therefore, the "single layer plug 42b" would include an interface between multiple vias, and the Office Action's rationale on page 6 that the device of the '357 reference does not exhibit any type of interface is unsupported. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness.

ISSUE 2: The §103(a) rejection of the claims is improper because hindsight is applied in view of the combination of the asserted teachings provided by way of the *Korman*'357 and *Green* '895 references.

The Examiner had applied improper hindsight in asserting that the claims are obvious under the requirements of §103(a) in view of the combination of asserted teachings, respectively provided by way of the '357 and '895 references. As set forth in

the Background portion of Appellants' Specification (page 2, line 4 through page 4, line 5 as well as page 6, line 24 through page 7 line 3), the claimed invention is directed to a semiconductor device which permits use of an aluminum-based via for interconnecting metal portions while also inhibiting structural defects such as flux divergence and electromigration degradation. This Background portion of Appellants' Specification explains that conventional metals used in this environment (such as tungsten) do not provide the same benefits as aluminum. Where attempts to implement aluminum vias have been made, semiconductor devices have suffered from the above-mentioned problems including flux divergence and electromigration degradation.

The asserted prior art does not recognized these problems set forth in Appellants' Specification and, as acknowledged in Examiner's Office Action (8/27/2002), fails to teach Appellants' device as claimed. To be clear, the Office Action does not advance the argument that the asserted prior art either recognizes or addresses the problems discussed by Appellants when conventional metals are used in this environment. Rather, the Examiner has very carefully attempted to read (independent claim 27) on the embodiment illustrated has figure 3 of the *Korman '357* reference. This *Korman '357* reference expressly indicates that the preferred material for its alleged corresponding via is not aluminum but rather is copper: each of layers 38,40 and 42 (including the material for the alleged corresponding via) "are preferably copper" along with metal pad 22 and copper post 36. (See, col. 5, lines 4-51). Use of copper material for these interconnects, allegedly corresponding vias and pads, is directly associated with the purpose of the alleged invention of the *Korman '357* reference; this purpose being "to provide a *FET array* [emphasis added] employing high density interconnect (HDI)" to overcome disadvantages of device element interconnections including excellent electrical conductivity. (See, col. 3, lines 5-27). HDI circuits do not employ the type of aluminum-based via structure as asserted in the Office Action. Moreover, while the *Green '895* reference may discuss various attributes of such available conductive metal materials, the *Korman '357* reference prefers copper over other conductive metal materials. Moreover, contrary to the suggestion in the Office Action, the *Green' 895* reference does not teach that copper and aluminum are interchangeable for either the above-discussed purpose of the *Korman '357* reference or for problems addressed in Appellants' Specification.

With that understanding of the invention and the has asserted prior art, Appellants respectfully submit that the Examiner has presented an argument of obviousness that cannot be maintained because: 1) the §103 rejection fails to include evidence of the alleged motivation to make the combination asserted in the Office Action; 2) the problems addressed by the cited prior art and the claimed invention are entirely different and thereby rebut any argument that the skilled artisan would be led to implement the modification as has asserted; and 3) a §103 rejection cannot be maintained when the rejection proposes a modification that undermines the purpose of the main reference, as it does in this instance for the purpose of the *Korman '357* reference.

With respect to the requisite evidence for the alleged motivation to make the combination has asserted in the Office Action, a significant body of authoritative case law clearly indicates that such evidence must be found in the prior art. For example, *Ruiz v. A.B. Chance Co.*, 234 F .3 654,57 U.S.P.Q.2d 1161 (Fed. Cir. 2000), indicates that the alleged motivation for combining the references is to be suggested by the references ("Our court has provided [that the] motivation to combine may be found explicitly or implicitly: 1) in the prior art references themselves; 2) in the knowledge of those of ordinary skill in the art that certain references, or disclosures in those references, are of special interest or importance in the field; or 3) from the nature of the problem to be solved, "leading inventors to look to references relating to possible solutions to that problem."). The Office Action cannot simply assert that an important claim limitation (such has aluminum) can be replaced based on an unsupported argument that, perhaps for some other purpose and in some other environment, the claim limitation being replaced is not so important and therefore is interchangeable for an unspoken purpose. In this instance, the Office Action is completely silent on the purpose for interchanging aluminum and copper which, by itself should be taken has an acknowledgement that the evidence is lacking.

With respect to the problems addressed by the cited prior art and the claimed invention, the M.P.E.P. and case law fully support the notion in the statute that the claim must be considered "as a whole" (35 U.S.C. §103(a)) which contemplates the problems discovered, discussed, and addressed by Applicant's claimed invention. See, for example,

M.P.E.P. §2141.02 which clearly indicates that discovering the source or cause of a problem is part of the "as a whole" inquiry; *see also In re Sponnoble*, 405 F.2d 578,585, 160 U.S.P.Q. 237,243 (CCPA 1969). In this instance, the Examiner has entirely ignored the problems discovered, discussed and addressed by Appellants' claimed invention and has also entirely ignored the problems being addressed by the prior art. As mentioned above and discussed more fully below, these problems being addressed by the prior art have nothing to do with the claimed invention and they cannot be disregarded when considering a modification to the prior art. Because of the lack of any such nexus in this regard, considering the claimed invention "as a whole" (as required by35 U.S.C.§ 103(a)), the Examiner's argument that the skilled artisan would- be led to implement the modification is clearly rebutted.

ISSUE 3: The §103(a) rejection of the claims is improper because the asserted modification of the primary *Korman*'357 reference would render that reference unsatisfactory for its intended purpose.

The § 103 rejection is improper because no §103 rejection can be maintained when the asserted modification undermines purpose of main reference. As stated in the Scope and Content of Prior Art, *Korman* '357 is applicable to the building an array of "one or more *off-the-shelf field effect transistors* [emphasis added] to form a package that compensates. . ."(lines 32 – 34, col. 3.) Thus, discrete FET elements are grouped and electrically connected together. In contrast, Appellants' claimed invention is directed to a monolithic IC design and the solving of its interconnection challenges, and is thus, not applicable to *Korman* '357. See, e.g., In re Gordon, 733 F.2d 900,221 U.S.P.Q. 1125 (Fed. Cir. 1984) when the asserted modification undermines purpose of main reference, the prior art teaches away and the rejection must be withdrawn). As discussed above, the Examiner's proposed modification undermines the purpose of the *Korman* '357 reference; therefore, the rejection cannot be maintained.

ISSUE 4: The §112(1) rejection is improper because the Specification describes the claimed subject matter in such a manner that one skilled in the art would be able to make and use the invention.

The Section §112, first paragraph rejections are improper because the Specification describes the claimed subject matter in such a manner that one skilled in the art would be able to make and use the invention. With respect to limitations in claims 28 -32 and 34, applicant submits that the examples discussed in connection with FIGs. 2A-2D show a plug 255 having attributes to which the claim limitations are directed. For example, when the dielectric material 230 is not polished using chemical mechanical polishing (CMP), it does not exhibit properties that would exist, had it been polished. Such characteristics of polished surfaces (*e.g.*, grain boundaries and surface conditions) are well known in the art. Similarly, the plug 255 does not exhibit limitations including: an interface formed when a first portion of a plug is planarized before a remaining portion; an interface formed when a first portion of the plug is subjected to CMP; an interface formed when a first portion of the plug is etched before forming a remaining plug portion; or grain boundaries that are formed at an internal interface between two plug portions formed by a separate process. Moreover, various portions of the specification discuss benefits of avoiding such attributes. For instance, page 3, lines 13-16 discusses difficulties with etching aluminum. Similarly, page 1, line 27 through page 2, line 1 discusses the need to planarize (*e.g.*, via CMP) or etch back excess metal, with grain boundaries inherently between firstly and secondly formed layers. In addition, the plug 255 would exhibit properties of an aluminum plug formed using a continuous deposition process in a single step when deposited aluminum is used for the plug, as described on page 10 lines 25-28 of the Specification. In view of the above, the §112, first paragraph rejections should be reversed.

ISSUE 5: The §112(2) rejection is improper because the Specification has concluded with claims particularly pointing out and distinctly claiming the subject matter which the Applicants regard as their invention.

The §112(2) is improper because the skilled artisan would recognize from the Specification that the claimed "single-layer plug" would not have the various interface problems/manifestations set forth in the rejected claims. Single-layer plugs that are made of aluminum inherently do not involve formation by two-step planarization (claim 28), intermediate-step CMP (claims 29 and 34), and grain boundaries formed by a two-step

process (claim 31). In addition, the Examiner rejection in the Final Office Action (8/27/2002) of the claims because the "essential structural cooperative relationships" that are not present, is improper. Specifically, the claims include negative limitations. Therefore, the cooperative relations are not required for the claimed subject matter. Therefore, the §112(2) rejections should be reversed. As noted by the Court *In re Swinehart*, 439 F.2d 210 USPQ 226 (CCPA 1971), "a claim may not be rejected solely because of the type of language used to define the subject matter for which patent protection is sought." Likewise, "breadth of a claim is not to be equated with indefiniteness." *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the claims, read in light of the specification, reasonably apprise those skilled in the art both of the utilization and scope of the invention, and if the language is as precise as the subject matter permits, 35 U.S.C. §112(2) demands no more. In view of above, the §112(2) rejection should be reversed.

IX. CONCLUSION

Appellant respectfully request reversal of the rejections as applied to the appealed claims and allowance of the application.

Please charge Deposit Account No. 14-1270 (PHA 51108A) in the amount of $320.00 for filing of a Brief in support of an appeal as set forth in 37 CFR §1.17(c).

Respectfully submitted,

By Peter Zawilski
Peter Zawilski
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Corporate Patent Counsel
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580 White Plains Road
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APPENDIX OF CLAIMS – 09/775,370

27. A semiconductor device comprising:

a first metal portion over a substrate;

a dielectric layer above the first metal portion;

a second metal portion above the dielectric layer;

a single-layer aluminum alloy plug extending from the first metal portion through the dielectric layer to the second metal portion, the plug having a first upper surface extending laterally beyond the second metal portion and substantially planar to an upper surface of the dielectric layer and a second upper surface that extends above the first upper surface.

28. The device of claim 27, wherein the single-layer plug does not exhibit an interface that would exist, were a first portion of the plug planarized before a remaining portion of the plug is formed.

29. The device of claim 27, wherein the single-layer plug does not exhibit an interface that would exist, were a first portion of the plug subjected to chemical mechanical polishing (CMP) before a remaining portion of the plug is formed.

30. The device of claim 27, wherein the single-layer plug does not exhibit an interface that would exist, were a first portion of the plug etched before a remaining portion of the plug is formed.

31. The device of claim 27, wherein the single-layer plug does not exhibit grain boundaries that would result from an internal interface between two portions of a plug formed during separate processes.

32. The device of claim 27, wherein the single-layer plug exhibits properties that are about identical to those exhibited by a single-layer aluminum alloy plug formed using a continuous deposition process.

33. The device of claim 27, wherein the dielectric layer is a single-layer dielectric.

34. The device of claim 33, wherein the dielectric layer has an upper surface that does not exhibit surface characteristics that would exist, were the upper surface planarized using CMP.

35. The device of claim 27, wherein the plug does not exhibit a void.

36. The device of claim 27, wherein the second upper surface of the single-layer plug is substantially planar with a second upper surface of the dielectric layer.

37. The device of claim 36, wherein a portion of the dielectric layer including the second upper surface has a side wall portion that is substantially aligned with a first side wall portion of the second metal layer, and wherein the portion of the plug including the second upper surface has a side wall portion that is substantially aligned with a second side wall portion of the second metal layer.